Sub-module component developed in CBuilder for MMC control and protection test in RTDS

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Abstract

Modular multilevel converter (MMC) is one of the most promising direct-current (DC) transmission modules. To establish a flexible sub-module model in RTDS for evaluating the protection and control devices is important and useful for the fast development of MMC-HVDC technology. A component for the sub-module, rtds_SM, is proposed in this paper, which is developed by CBuilder in RTDS to provide a flexible and available model to test the control and protection devices for MMC system. First, the rtds_SM component, considering the bypass switch branch, is established by using CBuilder in RTDS. It has seven inputs and two outputs, which can respond to various operation states under various conditions. The information of the capacitor voltage balancing is calculated in the component and output as a variable. Second, the memory usage and the simulation precision of the proposed model are analyzed in detail. It is suitable for the simulation in RTDS if the carrier frequency is smaller than 1.2 kHz. Third, the steady states and transient states are tested for the rtds_SM proposed in this paper. Numerical results show that it meets the requirements for various operating conditions. The proposed component has been successfully used to test the controller and protection devices designed by Xian XD Power Systems Co., Ltd. for a practical MMC system in China.

1. Introduction

With the development of renewable energy, VSC has been developing rapidly for its flexibility and high controllability [1, 2]. However, the conventional VSC, which is based on two-level or three-level converter [2], has high switching losses because of the high switching frequency. Moreover, the higher harmonics, the limited voltage level and the difficult voltage balancing between devices [3] are disadvantages of the conventional VSC system.

MMC has drawn much attention in recent years [4–11]. The flexible topology structure of MMC leads a way to solving the problems caused by the conventional VSC [4]. The study on MMC is mainly focused on the mathematical models [5–7], capacitor voltage balancing control [8–11] and modulation strategy [10–15].

An efficient MMC model based on time-varying Norton equivalent circuit [5] is proposed to reduce the number of the nodes for the calculation in simulation. A generalized mathematical model for MMC under balance and unbalance conditions is established by using sequence component method [6]. PD-SPWM strategy [8, 9] are proposed to solve the problems of voltage balancing. The capacitor voltage balancing is theoretically analyzed and an additional control is proposed in [10]. MPC is proposed to eliminate the circulating currents [11] by using the redundant switching states. The space vector PWM strategy for MMC [12, 13] is widely used for the modulation method of MMC system. The NLC [14] is proposed to reduce the THD.

The topology construction of the three-phase MMC is shown in Fig. 1. It contains 6 bridge arms and each arm consists of many SMs and a reactor, L, connected in series [4].

The main construction of SM is shown in Fig. 2. IGBT1 and IGBT2 are insulated gate bipolar transistors. D1 and D2 are antiparallel-connected diodes. C is the capacitance of the capacitor. Vc is the voltage of the capacitor. Vout is the output voltage of the SM.

There are two ways to establish the MMC system in RTDS: (1) Establish the MMC system with the small step components, and (2) Use the given components in RTDS to build MMC system.

For the former way, the network limitation for small-step systems in RTDS is 30 nodes and 36 switch devices [17]. That is, each bridge arm can only have two SMs in a small step encapsulation module at most.

For the latter way, there are three given components for MMC in RTDS: rtds_vsc_MMC4, rtds_vsc_CHAINV3 and FPGA based MMC model.
The rtds_vsc_MMC4 and rtds_vsc_CHAINV3 components are shown in Fig. 3.

The rtds_vsc_MMC4 and rtds_vsc_CHAINV3 cannot be used to analyze the behavior of the MMC when SMs fail. Furthermore, the rtds_vsc_MMC4 component can only be used in P5 cards.

The FPGA based MMC model is the latest component for MMC provided by RTDS Technologies Inc. The FPGA based MMC can support up to 512 SMs per arm and can represent some simple faults, such as the value change of the buffer reactor L, the value change of the capacitance of the capacitor and the bypass of the whole arm. However, many kinds of SMs' faults could not be represented by this model, such as: (1) the bypass switch refuses to act, (2) the thyristor after the rising edge shows up. The protective thyristor valve will be fired by the rising edge of the signal T. There would be several microseconds delay for the action of the bypass thyristor after the rising edge shows up. The protective thyristor switch is fired by the firing pulse T to reduce the current of D2 if necessary [16].

2.2. The model of capacitor

The relationship between the voltage and the current of the capacitor is:

\[ V_c(t) = \frac{1}{C} \int_0^t I_c(t) \, dt \]  

(1)

Linearizing (1) with the trapezoidal integration method [5],

\[ V_c(t) = V_c(t - dt) + \frac{dt}{2C} [I_c(t - dt) - I_c(t)] \]

(2)

Then,

\[ I_c(t) = \frac{2C}{dt} [V_c(t) - V_c(t - dt)] - \frac{2C}{dt} [V_c(t - dt) - V_c(t - 2dt)] \]

(3)

Therefore,

\[ I_c(t) = G_c V_c(t) + I_{b1}(t) \]

(4)

where \( I_{b1}(t) = -G_c V_c(t - dt) - I_c(t - dt) \) is the equivalent injective current source. \( G_c = 2C/dt \) is the equivalent conductance. \( dt \) is the simulation time step. Smaller \( dt \) leads to higher precision.

2.3. The model of IGBT

Assuming \( S_1 \) and \( S_2 \) are the switching functions of IGBT1 and IGBT2, respectively. \( S_1 (S_2) = 1 \) when IGBT1 (IGBT2) is switched on and \( S_1 (S_2) = 0 \) when IGBT1 (IGBT2) is switched off. When the IGBT is switched on, it equals to a small-value resistance \( R_{on} \), such as \( 10^{-5} \) \( \Omega \). When the IGBT is switched off, it can be considered as a large-value resistance \( R_{off} \), such as \( 10^5 \) \( \Omega \).

Therefore, the equivalent resistance \( R_{on} \) for the upper switch IGBT1 and the equivalent resistance \( R_{off} \) for the lower switch IGBT2 are,

\[
\begin{align*}
R_{on} &= S_1 \cdot R_{on} + S_2 \cdot R_{off} \\
R_{off} &= S_1 \cdot R_{off} + S_2 \cdot R_{on}
\end{align*}
\]

(5)

When the SM is inserted, the equivalent resistance of IGBT1 and IGBT2 are \( R_{on} \) and \( R_{off} \), respectively,

\[
\begin{align*}
R_{on} &= R_{on} \\
R_{off} &= R_{off}
\end{align*}
\]

(6)
When the SM is bypassed, the equivalent resistance of IGBT1 and IGBT2 are $R_{off}$ and $R_{on}$, respectively.

\[
\begin{align*}
R_{off} & = R_{1} \\
R_{on} & = R_{2}
\end{align*}
\]

2.4. Antiparallel-connected Diode Equivalent Model

Assuming that the $R_{D1}$ ($R_{D2}$) is equivalent resistance of D1 (D2), the value of $R_{D1}$ ($R_{D2}$) is determined by the potential difference of

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**Table 1**

<table>
<thead>
<tr>
<th>State of SM</th>
<th>Switch state</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Blocked</td>
<td>IGBT1 off, IGBT2 off</td>
<td>The capacitor can be charged through diode D1, but it cannot discharge.</td>
</tr>
<tr>
<td>Inserted</td>
<td>IGBT1 on, IGBT2 off</td>
<td>The capacitor can be charged through D1 or discharge through IGBT1.</td>
</tr>
<tr>
<td>Bypassed</td>
<td>IGBT1 off, IGBT2 on</td>
<td>The sub-module is bypassed through IGBT1 or D2, and the capacitor voltage remains constant.</td>
</tr>
</tbody>
</table>

**Fig. 3.** Existing MMC components.
**3. The rtds_SM component defined in CBuilder**

3.1. Equivalent circuit of SM

The software CBuilder in the package RSCAD provides a mechanism for researchers to develop their own components [17]. The Norton equivalent model should be used for all the defined components [17] in CBuilder. The equivalent circuit of a two-terminal element is shown in Fig. 7.

where \( g \) is the equivalent resistance. \( i_g(t) \) is the equivalent current source. \( v(t) \) and \( i(t) \) are the voltage and current of the branch.

In CBuilder, \( i_g(t) \) should be zero when \( g \) is very small. Otherwise, floating errors will occur when compiling the model in CBuilder.

According to the various states of IGBTs and Diodes, there are three operating modes of SM (see Table 3).

The corresponding equivalent circuits of these three modes are shown in Fig. 8.

3.2. The SM model established in CBuilder

To represent the behavior of the SM under various conditions, the rtds_SM component has seven inputs and two outputs.

In Fig. 9, \( K \) is the signal for the bypass switch. \( F_{p1} \) and \( F_{p2} \) are firing pulse for IGBT1 and IGBT2. \( S_{1F} \) and \( S_{2F} \) are fault signals of IGBT1 and IGBT2. \( K_F \) is the fault signal for the bypass switch. \( K_F = 1 \) means the switch refusing to act. \( V_c \) and \( V_{ctrl} \) are the outputs of the model. \( V_c \) is the capacitor voltages. \( V_{ctrl} \) is used for capacitor voltage balancing [15], which is calculated by,

\[
V_{ctrl} = A \cdot I_c \cdot (V_{ref} - V_c) \quad (10)
\]

The parameters of the SM component can be edited through the main menu and tabs of the rtds_SM component, as shown in Fig. 10.

3.3. The flowchart of the rtds_SM

When \( K \) is on, the corresponding SM operates in Mode 2. When \( K \) is off, the operating conditions for the SM are represented in Table 4.

**Table 3**

<table>
<thead>
<tr>
<th>Modes</th>
<th>( g )</th>
<th>( i_g(t) )</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>( 1/R_{on} + G_c )</td>
<td>( i_g(t) ) in (4)</td>
<td>The capacitor is charging or discharging</td>
</tr>
<tr>
<td>2</td>
<td>( 1/R_{on} )</td>
<td>0</td>
<td>Small resistance short circuit</td>
</tr>
<tr>
<td>3</td>
<td>( 1/R_{off} )</td>
<td>0</td>
<td>Large resistance open circuit</td>
</tr>
</tbody>
</table>

**Table 2**

<table>
<thead>
<tr>
<th>Diode operating condition</th>
<th>Potential condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>( R_{on} )</td>
<td>( R_{off} )</td>
</tr>
<tr>
<td>( R_{on} )</td>
<td>( R_{off} )</td>
</tr>
<tr>
<td>( V_{N1} &gt; V_{N2} ) and ( V_{N1} &gt; V_{Nc} )</td>
<td>( V_{N1} &gt; V_{N2} ) and ( V_{N1} &lt; V_{Nc} )</td>
</tr>
</tbody>
</table>

\*When \( R_{off} = R_{on} \) \( V_{sm} \) is only determined by \( R_{on} \) in spite of the state of \( D_{1} \).

**Fig. 4.** SM with protection circuit.

**Fig. 5.** Equivalent circuit when SM is blocked.

**Fig. 6.** Equivalent model of SM.

\( D_1 (D_2) \). When \( D_1 (D_2) \) is conductive, \( R_{D_1} (R_{D_2}) = R_{on} \). When \( D_1 (D_2) \) is blocked, \( R_{D_1} (R_{D_2}) = R_{off} \).

When SM is blocked (IGBT1 and IGBT2 are switched off), the SM equivalent circuit is shown in Fig. 5.

where \( N_1, N_2 \) and \( N_c \) are the name of each point. We use \( V_{N1}, V_{N2} \) and \( V_{Nc} \) to represent the potential of \( N_1, N_2 \) and \( N_c \). The equivalent resistance of \( D_1 \) and \( D_2 \) are shown in Table 2.

2.5. The model of SM

According to the analysis above, the basic equivalent model can be illustrated in Fig. 6.

where \( R_1 \) and \( R_2 \) are the equivalent resistance of the upper and lower arms in SM. The output voltage of SM is,

\[
V_{SM}(t) = \frac{R_2}{R_1 + R_2} V_c(t) \quad (8)
\]

where,

\[
\begin{align*}
R_1 &= E_N \cdot R_{1c} + (1 - E_N) \cdot R_{D_1} \\
R_2 &= E_N \cdot R_{2c} + (1 - E_N) \cdot R_{D_2}
\end{align*}
\]

\( E_N \) is used to enable the controller. If the firing pulses for IGBTs are blocked, \( E_N = 0 \); if not, \( E_N = 1 \). The details of \( E_N \) are explained in Section 4.4.

**Fig. 7.** Equivalent circuit of two-terminal equipment.

**Fig. 8.** Three modes equivalent circuit of two-terminal equipment.
The flowchart to establish the rtds_SM component in CBuilder is shown in Fig. 11.

In Fig. 11, $P_S$ is calculated by the value of $K$ and $K_F$. If the switch is on, $P_S = 0$; if the switch is off, $P_S = 1$.

$E_N$ is used instead of setting both $F_{P1} = 0$ (IGBT1 is off) and $F_{P2} = 0$ (IGBT2 is off) to confirm whether the SM operates under the correct mode. The “Combination Mode” shown in Fig. 11 represents the situation when $E_N$ is 1 and the SM switches between Mode 1 and Mode 2.

### 3.4. The function of the enable signal $E_N$

In RTDS, if the frequency of the firing pulse is less than 500 Hz, the $F_{P1}$ and $F_{P2}$ may not switch at the same time, as shown in Fig. 12.

Though the SM does not operate on $F_{P1} = 0$ and $F_{P2} = 0$ in practice, it can be seen that the $F_{P1}$ and $F_{P2}$ will both be 0 at the same time in one circle in RTDS simulator. If we use $F_{P1} = 0$ and $F_{P2} = 0$ to detect if the SM is blocked and enter the “Combination Mode”, the curve of $V_{sm}$ would be (see Fig. 13).

$E_N$ is proposed to solve the problem when the frequency of the firing pulse is less than 500 Hz in RTDS. When $E_N = 0$, the firing pulses of IGBT1 and IGBT2 are blocked. On the contrary, when $E_N = 1$, the firing pulses are unblocked.

The curve of $V_{sm}$ is improved by using $E_{P1}$. However, if the frequency of the firing pulse is more than 500 Hz, the calculating process is also correct without the $E_N$ (see Fig. 14).

$E_N$ can be obtained by two ways: (1) If the controller could provide the signal $E_N$ to the rtds_SM component, it can be directly used as an input of the rtds_SM. (2) If the controller could not provide the signal $E_N$, we can calculate $E_N$ by

$$E_N(t) = E_{P1}(t) + E_{P2}(t) + F_{P1}(t) + F_{P2}(t)$$

(11)

where the superscript ‘(t)’ and ‘(t – 1)’ represent that the corresponding value is of the current time instant and the last time instant respectively.

### Table 4

<table>
<thead>
<tr>
<th>IGBT1</th>
<th>IGBT2</th>
<th>$N_1$, $N_2$ and $N_C$</th>
<th>Operating mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>Off</td>
<td>Off</td>
<td>$V_{N1} &gt; V_{N2}$ and $V_{N1} &gt; V_{Nc}$</td>
<td>Mode 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{N1} &lt; V_{N2}$</td>
<td>Mode 3</td>
</tr>
<tr>
<td>On</td>
<td>Off</td>
<td>$V_{N1} &gt; V_{N2}$</td>
<td>Mode 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{N1} &lt; V_{N2}$</td>
<td>Mode 2</td>
</tr>
<tr>
<td>Off</td>
<td>On</td>
<td>–</td>
<td>Mode 2</td>
</tr>
</tbody>
</table>

Fig. 9. The icon of the rtds_SM component.

Fig. 10. Main menu and tabs of the rtds_SM component.

Fig. 11. Flowchart to realize the rtds_SM component in CBuilder.

Fig. 12. $F_{P1}$ and $F_{P2}$ when firing pulse frequency is 200 Hz.
3.5. The “Combination Mode”

When the “Combination Mode” is entered, the SM operates between Mode 1 and Mode 2 according to the state of IGBT1 and IGBT2. The shadow part “Combination Mode” in Fig. 11 is shown in Fig. 15.

The TEM_P is used to avoid wrong updating of the voltage of capacitor. When the SM operates in Mode 1, the model of the SM is shown in Fig. 7 and there are,

\[ V_c(t) = \frac{V_{N1}}{C_0} - \frac{V_{N2}}{C_0} \]
\[ I_c(t) = G_c V_c(t) + I_h(t) \]  

(12)

When the SM operates in Mode 2, the model of the SM is a small resistance and \( V_{N1} \) and \( V_{N2} \) are almost the same. The voltage of the capacitor keeps constant. When the mode of SM changes from Mode 2 to Mode 1, if there is no TEM_P and we use (12) for Mode 1, the voltage of the capacitor will change to zero at the first point because \( V_{N1} \) almost equals to \( V_{N2} \) at that point. Therefore, the output voltage \( V_c \) of the corresponding SM would be periodically charging from 0 at the point when the SM switches from Mode 2 to Mode 1, as shown in Fig. 16. As a result, the capacitor current increases sharply when its voltage suddenly drop to zero.

TEM_P can help the rtds_SM to maintain the capacitor voltage at the moment when the SM changes from Mode 2 to Mode 1. TEM_P is used to find out the point when SM changes from Mode 2 to Mode 1. At the switching point, \( V_c \) is not updated to \( V_{N1} - V_{N2} \). The former value of \( V_c \) is used to calculate for the first step and then it is calculated by using (12).

4. The memory usage and the simulation precision

4.1. Memory usage of rtds_SM component

The memory usage of every defined component in CBuilder is about 1/20 calculation capacity of GPC card, as shown in Fig. 18.

Considering the memory usage of the network solution and the limitation of the number of nodes, the number of GPC card for \( N + 1 \) levels of MMC system can be calculated by,

\[ N = \frac{6 \times 2}{20} = 0.6N \]

(13)

For PB5 card, we have,

\[ N = \frac{6 \times 2}{20 \times 1.2} = 0.5N \]

(14)

If the users only want to test the normal operation of MMC system, the rtds_vsc_MMC4 or rtds_vsc_CHAINV3 is good choice for less calculation capacity. However, if the users want to establish a MMC system to study their protection devices for MMC or control strategy for MMC, the proposed rtds_SM in RTDS is a better choice. The individual submodule model provides more flexible application than the given MMC integer bridge. It also needs much less memory than small-step system.

By using the proposed rtds_SM component, the following events in Table 5 can be simulated in RTDS for protection device detection, optimizing the control parameter and so on.

The proposed rtds_SM component can be used for many other tests in RTDS with the various inputs and parameters of each rtds_SM.

4.2. Simulation precision of rtds_SM component

The principle of firing pulse generated by using triangular carrier and sinusoidal modulation wave is shown in Fig. 19.
If all the lengths of the firing pulse intervals are longer than the simulation time step, the simulation time step is available for the system.

The shortest firing pulse interval is determined by the following three key factors: the intersection point, the carrier frequency and the modulation index.

4.2.1. The intersection point
The firing pulse interval changes with the intersection points of modulation wave and carrier wave, as shown Fig. 20.

If the time instances of the peak points of the modulation wave and carrier wave are same, we assume that the corresponding firing pulse time interval is $D_{tst}$. It can be seen that under the same carrier frequency and the same modulation index, the firing pulse interval $D_t$ is no less than $D_{tst}$.

4.2.2. Carrier frequency
The greater the carrier frequency, the shorter the firing pulse interval is. Assume that the ratio of the carrier wave frequency to the modulation wave frequency is $a$. The relationship between $D_{tst}$ and $a$ is shown in Fig. 21, when the modulation index is 1.0.

4.2.3. Modulation index
The greater the modulation index, the shorter the firing pulse interval is. The modulation index is usually smaller than 1 [19].

For $a = 25$ (the carrier frequency is 1.25 kHz), the relationship between $D_{tst}$ and the modulation index is shown in Fig. 22.

---

Table 5
The events can be supported by RTDS_SM component.

<table>
<thead>
<tr>
<th>Events description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 Start procedure</td>
</tr>
<tr>
<td>2 Stop procedure</td>
</tr>
<tr>
<td>3 A single SM faults and runs out of operation</td>
</tr>
<tr>
<td>4 Multiple SM fault and run out of operation</td>
</tr>
<tr>
<td>5 The redundant SM takes place of the blocked SM</td>
</tr>
<tr>
<td>6 We can set several redundant SM as we need</td>
</tr>
<tr>
<td>7 The behavior of the SM when K switches normally</td>
</tr>
<tr>
<td>8 The behavior of the SM when K is refused to switch</td>
</tr>
<tr>
<td>9 The behavior of the SM when IGBTs fault</td>
</tr>
</tbody>
</table>

---

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When the modulation index $M$ is smaller than 0.88 at $a = 25$ (the carrier frequency is 1.25 kHz), the shortest firing pulse interval $\Delta t_{\text{st}}$ is more than 50 $\mu$s.

Consequently, the proposed rtds_SM component is suitable for the simulation in RTDS if the carrier frequency is smaller than 1.2 kHz. If the carrier frequency is more than 1.25 kHz,
the suitable range of the modulation index is from 0 to less than 0.88.

5. Numerical tests

5.1. Single-phase two-Level test system

A single-phase two-level test system is established in RTDS as shown in Fig. 23. Each bridge arm of the system consists of a single rtds_SM component. The SM is fired by the pulse wave with 100 Hz and 0.5 duty cycle. The phase voltage magnitude is 2.5 kV and the initial phase angle is $\frac{\pi}{176}$. The fundamental frequency is 50 Hz.

To compare the simulation results with PSCAD, we build the same system in PSCAD as shown in Fig. 24. The voltage and current of the capacitor, the current of the upper arm and the voltage of the middle point between upper and lower arms are shown in Fig. 25.

5.2. Three-phase seven-level test system

A three-phase seven-level test system is established in RTDS and the carrier phase shift modulation method is used in this case. The parameters are shown in Table 6. The carrier phase-shifted modulation (CPS-SPWM) method is used in this case and the carrier frequency is 200 Hz.

5.2.1. The steady state simulation

The start procedure of the MMC-HVDC system is divided into two stages: uncontrolled stage and controlled stage. During the uncontrolled stage, the capacitors of SMs are charged with all IGBTs blocked. The controller is enabled at the beginning of the controlled stage.

The rtds_SM works well in the start procedure. During the uncontrolled start stage, the maximum voltage of the capacitors would be,

$$U_{c_{\text{max}}} = \sqrt{2}U_s / 6 = \sqrt{2} \times 10 / 6 = 2.36 \text{kV} \quad (15)$$

For the start procedure, the capacitor voltages in the upper arm of phase $a$ are shown in Fig. 26. $t_{st} = 0.182$ s is the end time for the uncontrolled stage. The controller is enabled at $t_{st}$ and the controlled stage starts. SMs are blocked before $t_{st}$. From $0 \sim t_{st}$, the capacitor is charged with IGBTs blocked. The capacitor voltages in an arm are almost same and their maximum capacitor voltages are decided by $U_s$, as shown in (15). At $t_{st}$, the controller is enabled by $E_N$. The uncontrolled stage is over and the controlled stage starts. During the controlled stage, the SMs are charged or discharged according to the different states of the IGBTs, as listed in Table 4. The simulation results of SMs’ capacitor voltages around $t_{st}$ are shown in Fig. 26.

By the effect of the controller, the capacitor voltages are adjusted to their rating values gradually. The capacitor voltages of SMs under controller of the upper arm in phase $a$ are illustrated as $V_c$ in Fig. 27. The output alternating voltage of phase $a$ ($V_{ba}$), the currents of the upper and lower arms in phase $a$ ($I_{ba}$ and $I_{bl}$), and the DC current ($I_{dc}$) are also shown in Fig. 27.

For the CPS-SPWM method, the output $V_{ctrl}$ is used for the voltage balancing control. Taking the 1st SM for example, the capacitor voltage $V_{ca1}$, the firing pulse $F_{p1}$ for IGBT1, and the balancing control variable $V_{cal}$ are shown in Fig. 28.

5.2.2. The transient state simulation

Assuming that the IGBT1 in the 6th SM (SM6) of the upper arm in phase $a$ cannot be triggered by the firing pulse at $t = 1.5$ s. IGBT2

$$V_{ca1}$$

Fig. 26. Capacitor voltage during the start procedure.
should be blocked when the fault happens to avoid the simultaneous conduction of IGBT1 and IGBT2. After 5 ms delay, the bypass switch of SM6 is turned on and a spare SM is put into operation at \( t_2 = 1.51 \text{ s} \) to restore the balance and stability of the system.

As shown in Fig. 29, \( S_{1F} \) and \( S_{2F} \) represent the states of IGBT1 and IGBT2 in SM6. \( V_{cau6}, K_{au6} \) and \( S1_{Fau6} \) are the capacitor voltage, bypass switch state and IGBT fault signal of SM6.

The DC side voltage and the alternating current of phase \( a \) are shown in Fig. 30. The capacitor of the spare SM starts to be charged when \( t_2 = 1.51 \text{ s} \), it needs about 0.1 s for the spare SM to reach its reference capacitor voltage.

It can be seen that the proposed rtds_SM component can be used for both various steady states and transient states. By using the 7 inputs signals, many kinds of faults for each SM and the faults combination can be implemented by using the proposed rtds_SM component. It can be used flexibly to test the protection devices and control strategies.

6. Conclusion

The existing model in RTDS, such as rtds_vsc_MMC4 and rtds_vsc_CHAINV3, cannot be used to analyze the behavior of SM or MMC when fault happens. To solve this problem, we propose a novel component, rtds_SM, which is developed in CBuilder software for RTDS simulation. It can be utilized to test the valves control and protection devices. The proposed component can represent various states of SM. Besides, the proposed rtds_SM component has the following favorable properties:

1. The proposed model includes not only the capacitor and IGBTs, but also the protection bypass switch \( K \) and the anti-parallel-connected diodes \( D_1 \) and \( D_2 \).
2. The individual sub-module model provides more flexible operation modes than the existing MMC bridges in RTDS. It can represent the behavior for various kinds of faults in SM and MMC.
3. It is suitable for the simulation in RTDS if the carrier frequency is smaller than 1.2 kHz. If the carrier frequency is more than 1.25 kHz, the suitable range of the modulation index is from 0 to less than 0.88.

The memory usage of rtds_SM is only 1/20 calculation capacity of GPC card. It needs much less memory usage than small-step system. To expand the scale of the simulation system, we commend that for the two-terminal MMC system, one side MMC converter can be modeled by using the proposed rtds_SM components and another side MMC converter can be established by using rtds_vsc_MMC4 or rtds_vsc_CHAINV3. The two converters could connect together through the interface transformer and transmission lines.

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References


